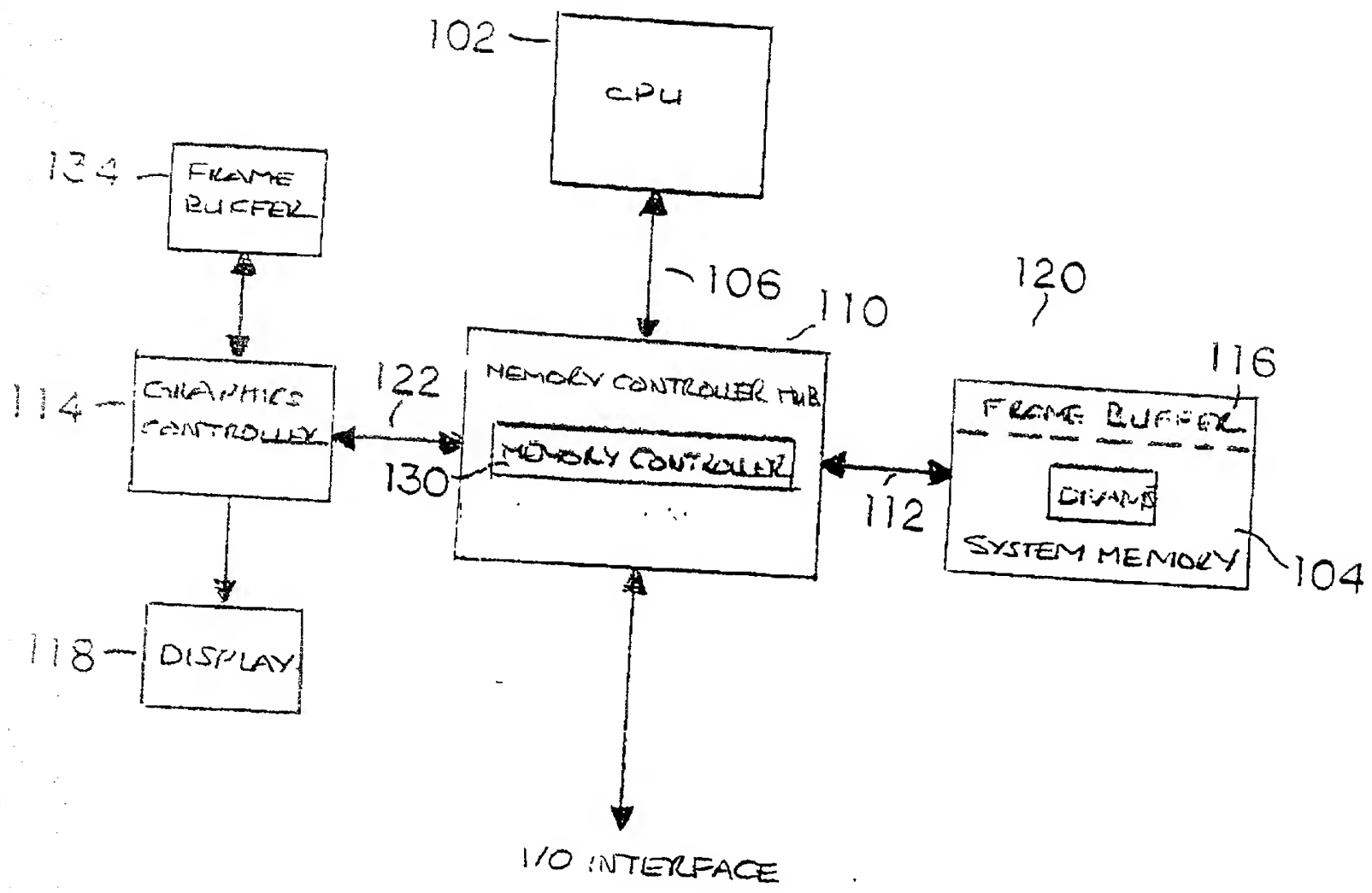
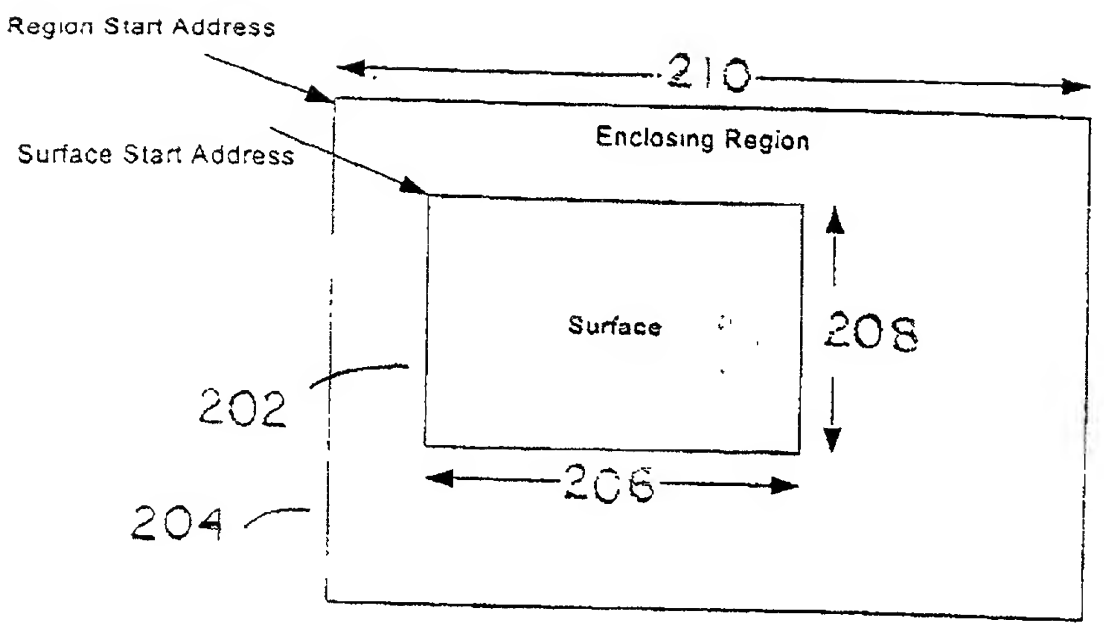

102
CPU
124
FRAME BUFFER
106
110
120
116
114
GRAPHICS CONTROLLER
122
MEMORY CONTROLLER HUB
130
MEMORY CONTROLLER
112
FRAME BUFFER
DRAM
SYSTEM MEMORY
104
118
DISPLAY
I/O INTERFACE

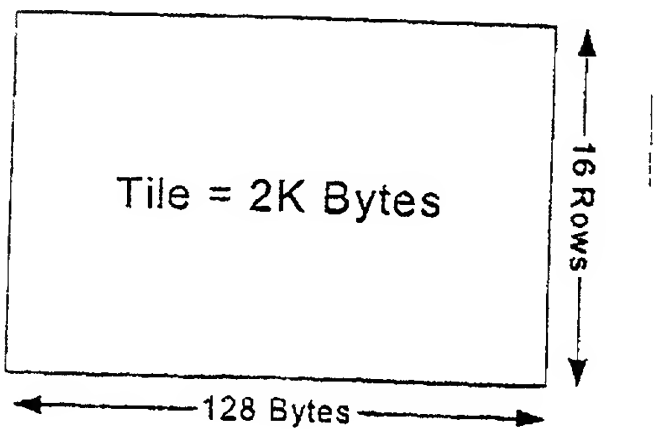
100

FIG. 1



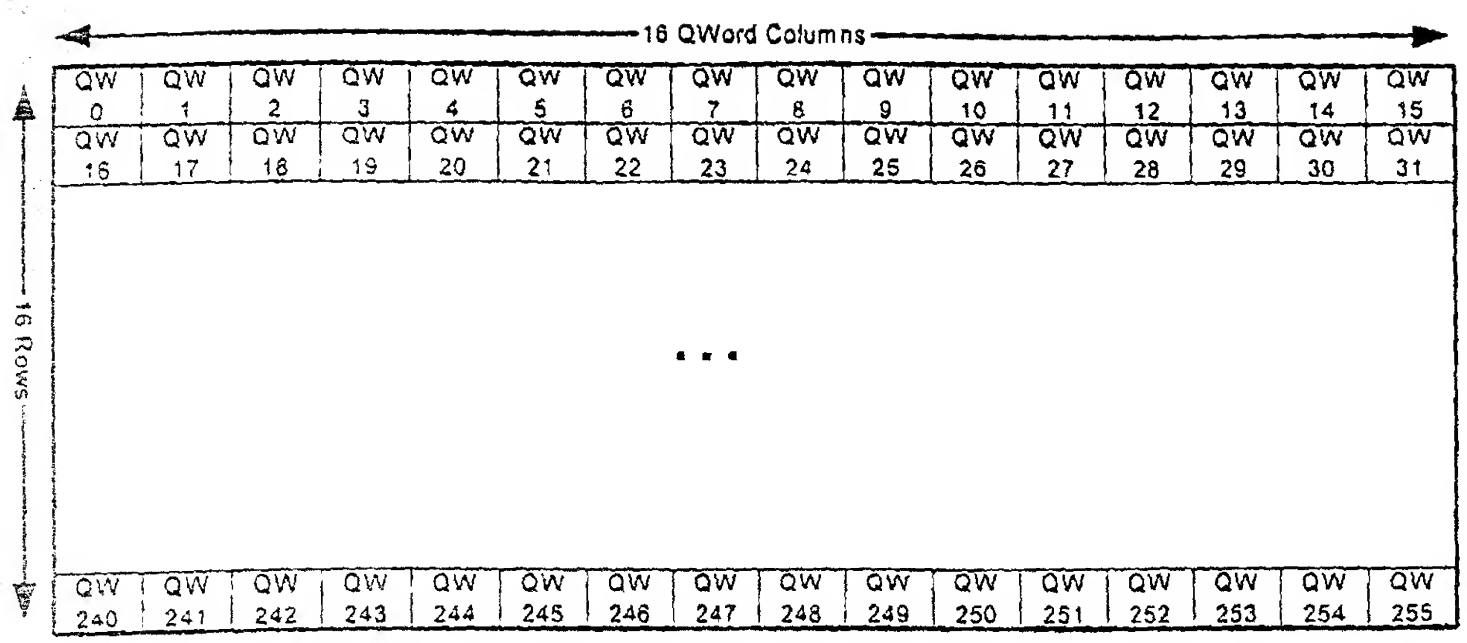
200

FIG. 2(a)



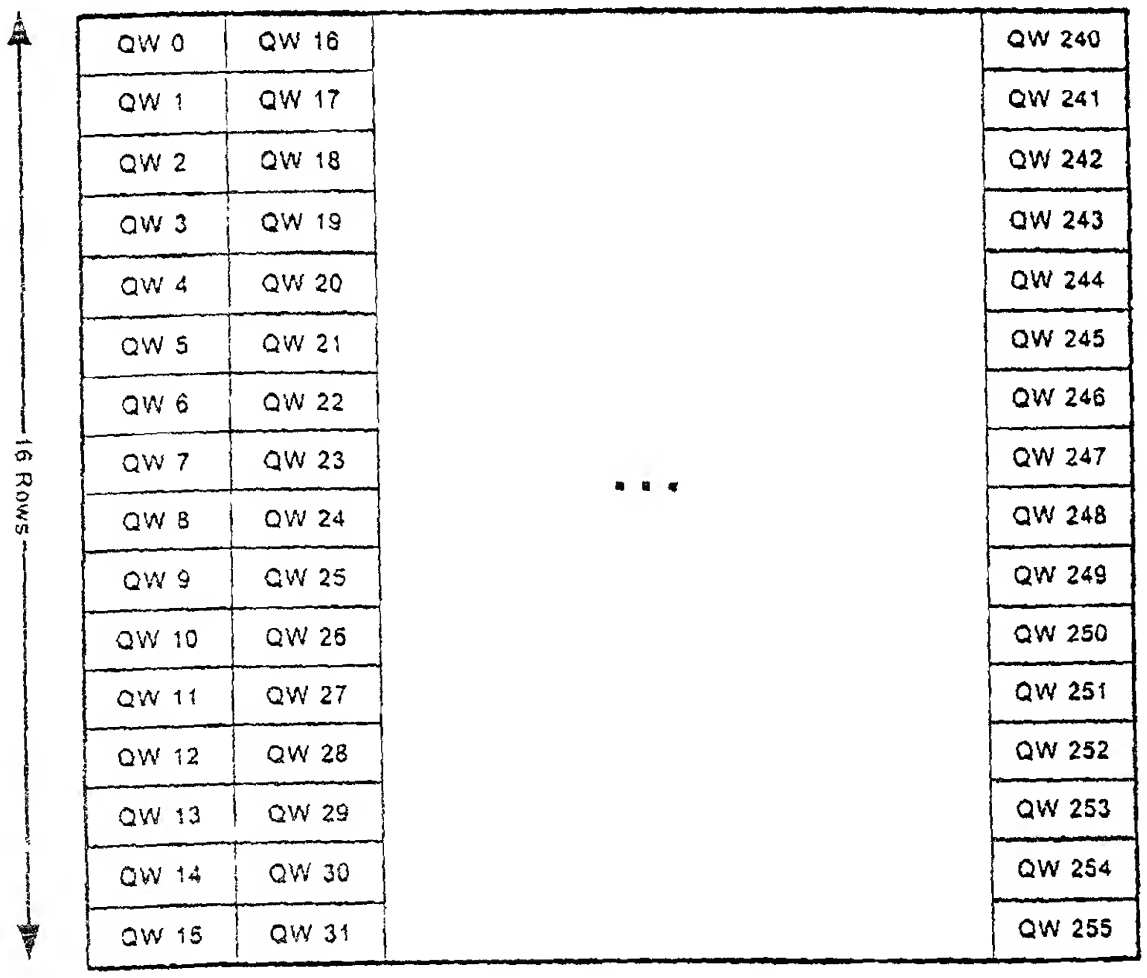
212

FIG. 2(b)



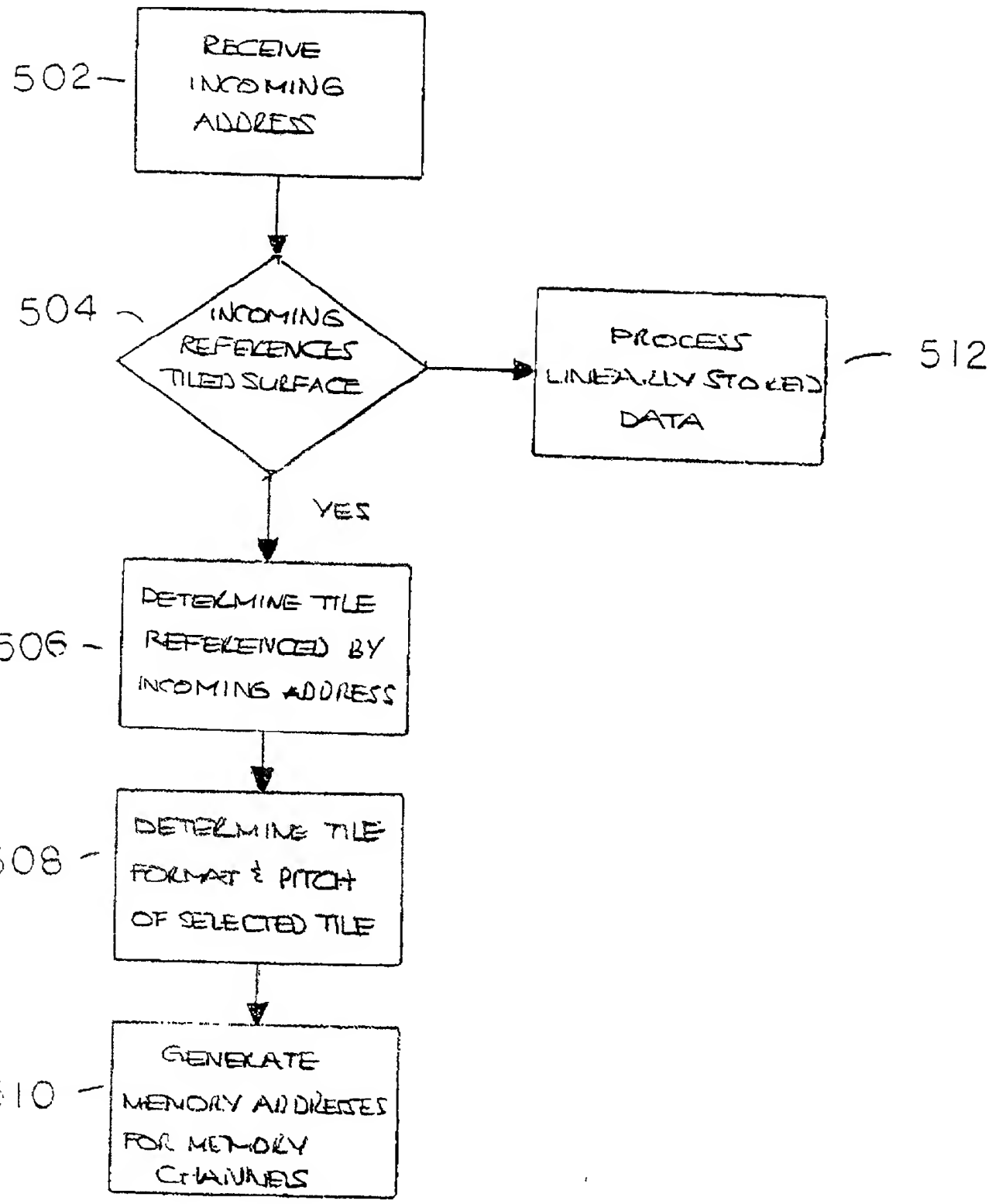
300

FIG. 3



400

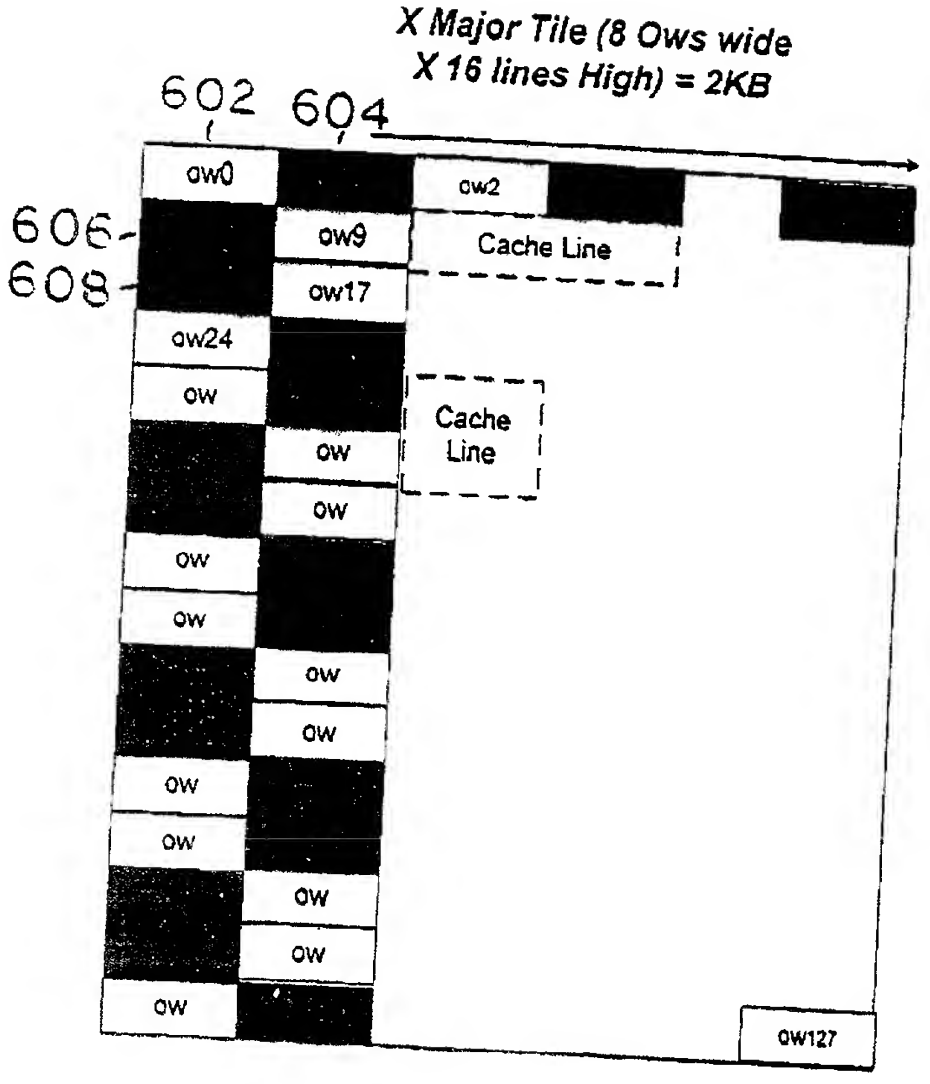
FIG. 4



500

FIG. 5

Received: 12/27/01 03:56PM



600

FIG. 6

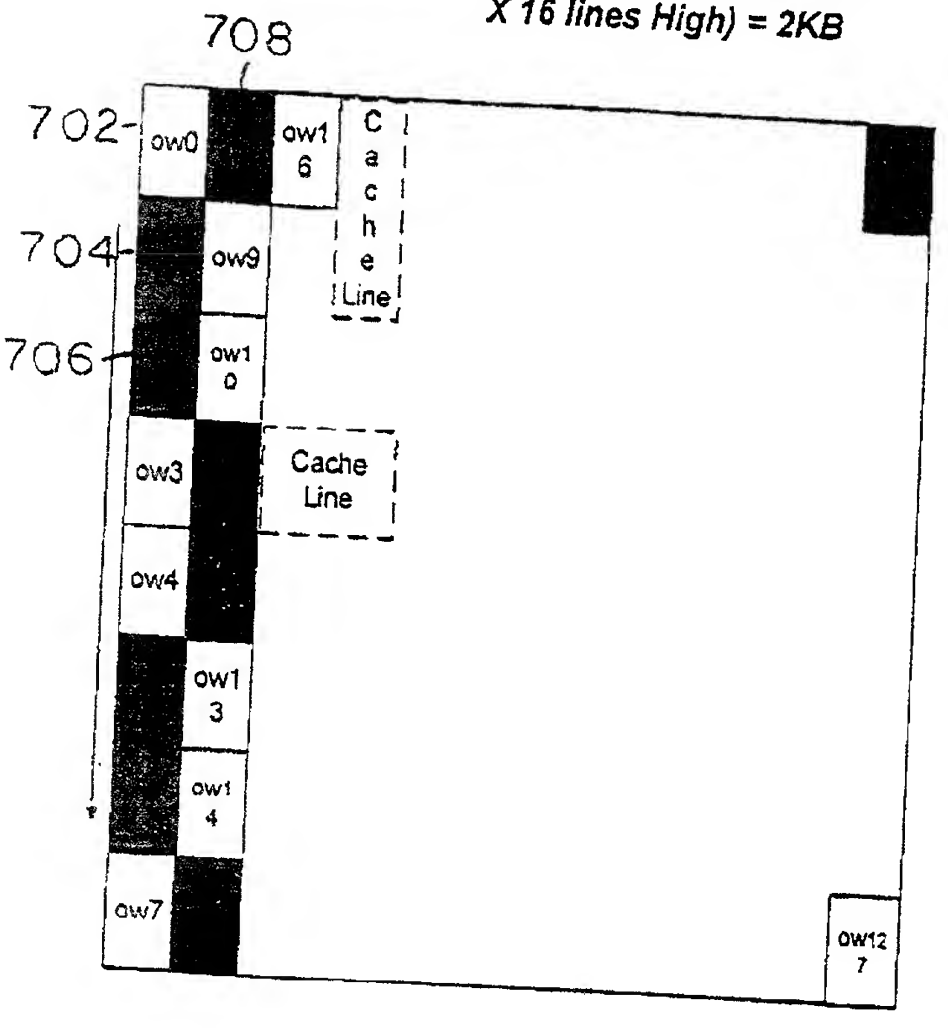
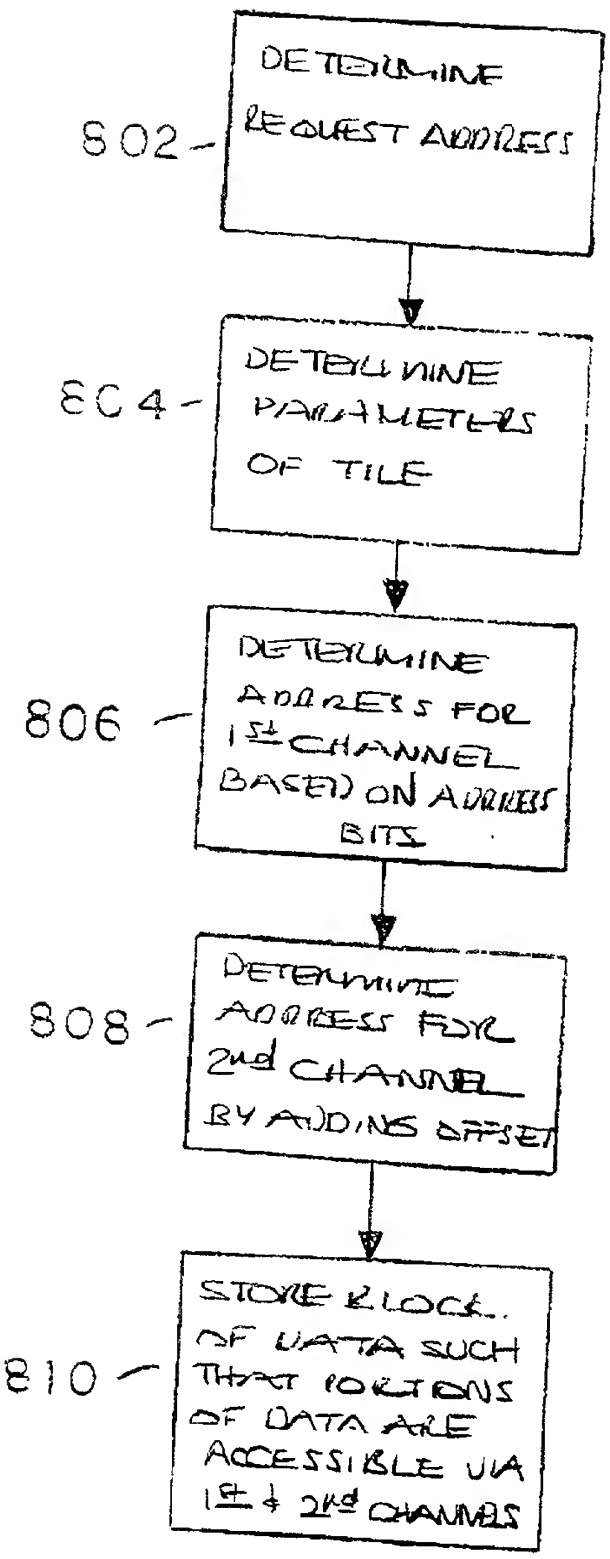


FIG. 7

700


802
DETERMINE REQUEST ADDRESS
804
DETERMINE PARAMETERS OF TILE
806
DETERMINE ADDRESS FOR 1st CHANNEL BASED ON ADDRESS BITS
808
DETERMINE ADDRESS FOR 2nd CHANNEL BY ADDING OFFSET
810
STORE BLOCK OF DATA SUCH THAT PORTIONS OF DATA ARE ACCESSIBLE VIA 1st & 2nd CHANNELS

800

FIG. 8

Request Address (31:5) = Translated Tiled Address (31:5)

If (Tiled Addr [8] == '0' AND Tiled Addr [7] =='0') OR
(Tiled Addr [8] == '1' AND Tiled Addr [7] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 16B

If (Tiled Addr [8] == '0' AND Tiled Addr [7] =='1') OR
(Tiled Addr [8] == '1' AND Tiled Addr [7] =='0'):
Channel 0: Request Address + 16B
Channel 1: Request Address

FIG. 9

Request Address (31:5) = Translated Tiled Address (31:5)

If (Tiled Addr [4] == '0' AND Tiled Addr [8] =='0') OR
(Tiled Addr [4] == '1' AND Tiled Addr [8] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 128B

If (Tiled Addr [4] == '0' AND Tiled Addr [8] =='1') OR
(Tiled Addr [4] == '1' AND Tiled Addr [8] =='0'):
Channel 0: Request Address + 128B
Channel 1: Request Address

FIG. 10

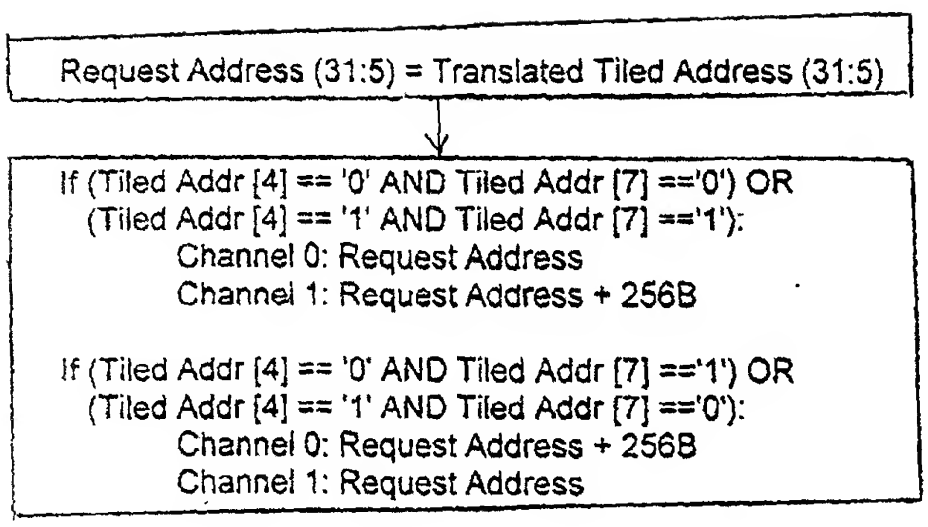

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [4] == '0' AND Tiled Addr [7] =='0') OR
(Tiled Addr [4] == '1' AND Tiled Addr [7] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 256B
If (Tiled Addr [4] == '0' AND Tiled Addr [7] =='1') OR
(Tiled Addr [4] == '1' AND Tiled Addr [7] =='0'):
Channel 0: Request Address + 256B
Channel 1: Request Address

FIG. 11

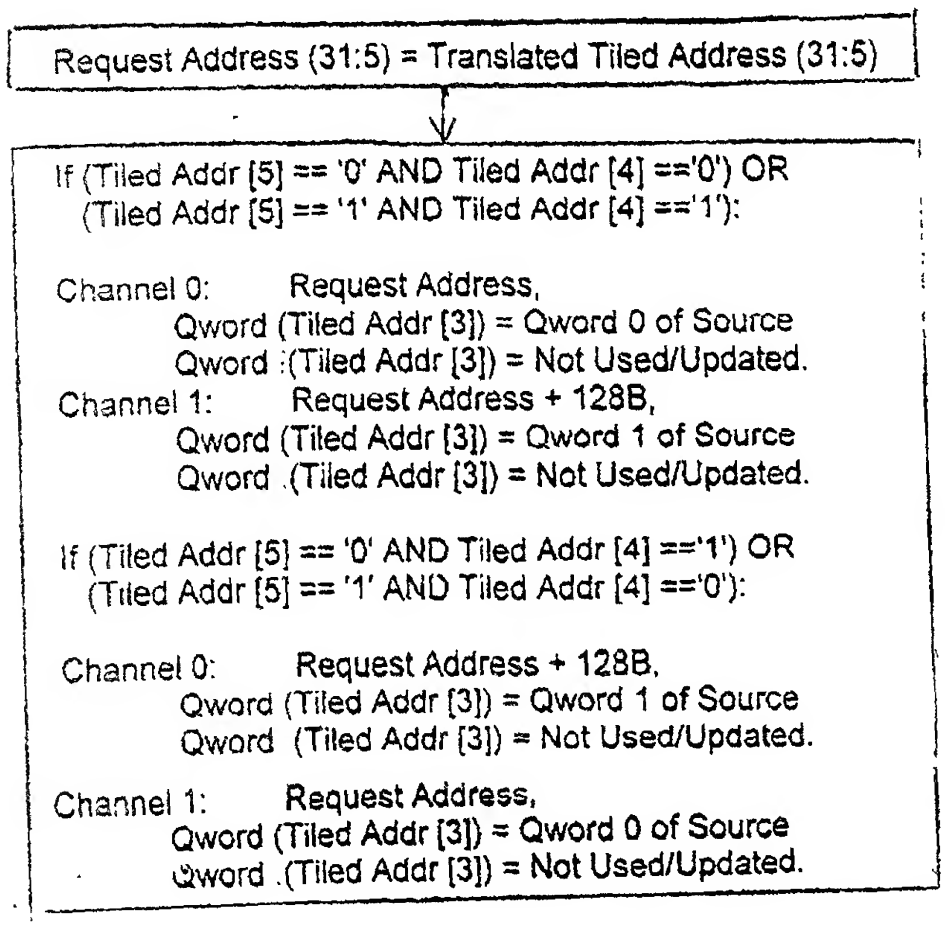

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='0') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='1'):
Channel 0: Request Address,
Qword (Tiled Addr [3]) = Qword 0 of Source
Qword :(Tiled Addr [3]) = Not Used/Updated.
Channel 1: Request Address + 128B,
Qword (Tiled Addr [3]) = Qword 1 of Source
Qword .(Tiled Addr [3]) = Not Used/Updated.
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='1') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='0'):
Channel 0: Request Address + 128B,
Qword (Tiled Addr [3]) = Qword 1 of Source
Qword (Tiled Addr [3]) = Not Used/Updated.
Channel 1: Request Address,
Qword (Tiled Addr [3]) = Qword 0 of Source
Qword .(Tiled Addr [3]) = Not Used/Updated.

FIG. 12

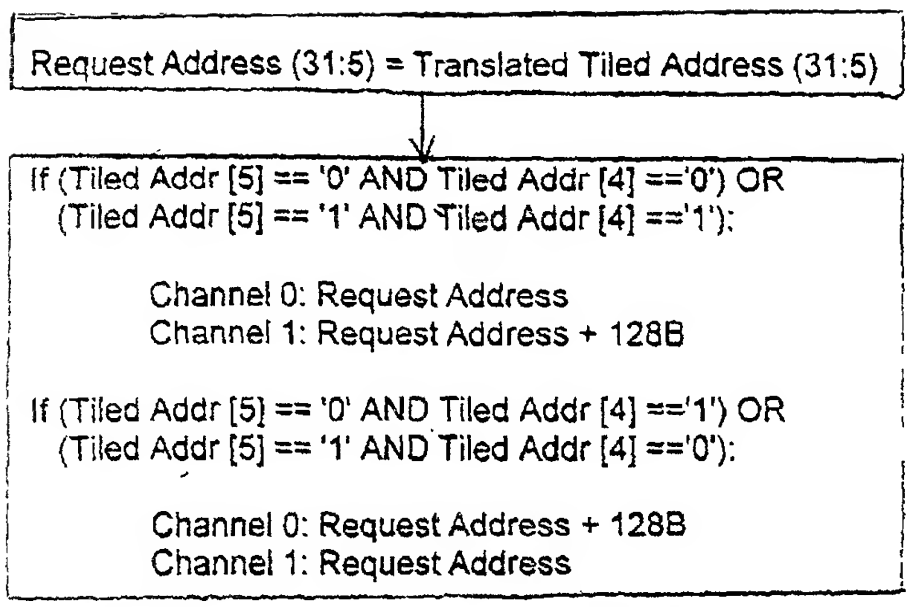

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='0') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 128B
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='1') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='0'):
Channel 0: Request Address + 128B
Channel 1: Request Address

FIG. 13

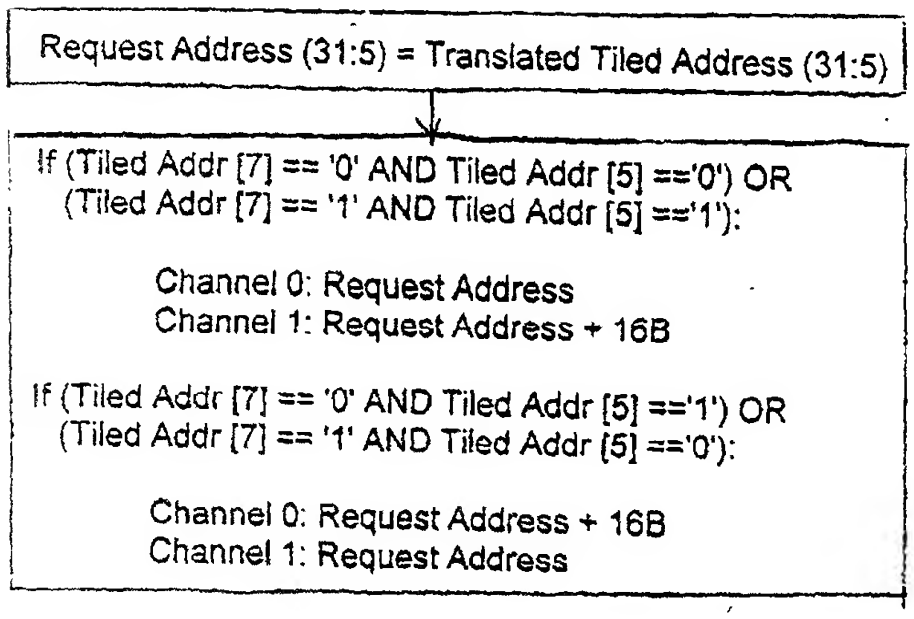

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [7] == '0' AND Tiled Addr [5] =='0') OR
(Tiled Addr [7] == '1' AND Tiled Addr [5] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 16B
If (Tiled Addr [7] == '0' AND Tiled Addr [5] =='1') OR
(Tiled Addr [7] == '1' AND Tiled Addr [5] =='0'):
Channel 0: Request Address + 16B
Channel 1: Request Address

FIG. 14